Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.0095”**

**.019”**

**.019”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0095”**

**Backside Potential: CATHODE**

**Mask Ref: TSO**

**APPROVED BY: DK DIE SIZE .019” X .019” DATE: 11/10/22**

**MFG: ALLEGRO / SPRAGUE THICKNESS .007” P/N: 1N3070**

**DG 10.1.2**

#### Rev B, 7/1